Variable Dynamic Range CMOS Image Sensor with Area-Efficient LOFIC Pixel and Readout Circuit

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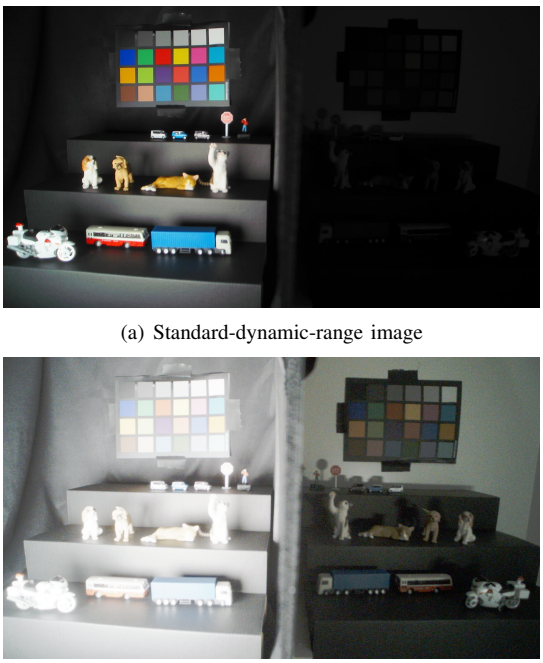
***Abstract*—Single exposure high-dynamic-range (HDR) image sensors have been developed to capture moving objects under extreme illumination conditions. The lateral overflow integration capacitor (LOFIC) pixel structure is considered as one of the solutions. However, the required dynamic range varies depending on the scene, and an excessively high dynamic range can lead to contrast degradation. To achieve an HDR CMOS image sensor with a variable dynamic range, we propose an area-efficient variable pixel and a corresponding readout circuit. The variable pixel supports three photo-electron conversion gains by controlling the bottom plate voltage of the overflow capacitor, thus the pixel size can remain as small as that of a conventional LOFIC pixel. The readout double sampling (DS) circuit processes polarity-inverted high-conversion-gain (HCG) and low-conversion-gain (LCG) signal. As a result, the dynamic range can be varied across three HDR modes depending on the scene. The highest dynamic range is comparable to that of the conventional LOFIC pixel, while the conversion gain can be reduced by 13.3 dB or 18.1 dB to enhance image contrast.**

***Index Terms*—CMOS image sensor, LOFIC, HDR, High contrast, readout circuit, High SNR, variable conversion gain.**

I. Introduction

CMOS image sensors (CISs), when used under extreme illumination conditions such as outdoor environments, require high-dynamic-range (HDR) imaging technology to prevent underexposure and overexposure of objects within a scene. In order to realize HDR CISs, many approaches have been proposed, such as logarithmic compression [1], [2], multiple-exposure HDR (MEHDR), dual conversion-gain (DCG) pixels [3], [4] and lateral overflow integration capacitor (LOFIC) pixels [5]–[8]. The LOFIC pixel is promising for its linear response and reduced motion artifacts, in which the low-conversion-gain (LCG) signal to handle large maximum signal charges and high-conversion-gain (HCG) signal to reduce dark noise are combined. The LOFIC pixel is composed of typical 4 transistors, an overflow capacitor (C_S) and a switching gate (ΦSG). During HCG mode, when ΦSG is set to low, the dark signal charge integrated in a photodiode (PD) is read out with low input-referred noise thanks to the high conversion gain determined by the floating diffusion capacitance, C_{FD}. Conversely, during LCG mode, when ΦSG is set to high, the bright signal charge integrated in both the PD and C_S is read out to extend the full well capacity (FWC), which is primarily determined by C_S. Thus, the dynamic range is typically determined by the capacitance ratio of C_S to C_{FD}, which is fixed once the LOFIC CIS is designed and fabricated. For the LOFIC CIS, smaller C_S and larger C_{FD} are required to realize higher dynamic range. However, the required dynamic range varies depending on the scene, and an excessively high dynamic range can lead to contrast degradation. For instance, an image taken in standard-dynamic-range (SDR) mode, as shown in Fig. 1(a), exhibits good contrast for objects located on the bright left side, even though objects located on the dark right side are barely visible. In contrast, an image taken in HDR mode, as shown in Fig. 1(b), displays poor contrast overall, while all objects located in both the bright and dark areas are visible.



(a) Standard-dynamic-range image

(b) High-dynamic-range image

Fig. 1. Standard-dynamic-range image and High-dynamic-range image

This paper proposes a variable dynamic range CIS with an area-efficient pixel. Three photo-electron conversion gains—HCG (high-conversion-gain), MCG (middle-

TABLE I
COMBINATIONS OF THE PIXEL CONVERSION GAIN AND THE READOUT CIRCUIT MODE

mode	pixel conversion gain	readout circuit
HCG1	(1) HCG	(4) INV-AMP
HCG2	(2) MCG	(4) INV-AMP
LCG1	(2) MCG	(5) ATN
LCG2	(3) LCG	(5) ATN

TABLE II
VARIABLE HDR MODE FOR THE HCG AND LCG COMBINATION.

HDR mode	HCG	LCG
HDR1	HCG1	LCG1
HDR2	HCG1	LCG2
HDR3	HCG2	LCG2

conversion-gain), and LCG (low-conversion-gain)—can be selected, even though the pixel does not require additional transistors compared to the conventional LOFIC pixel. The proposed CIS also employs an area-efficient readout circuit that processes polarity-inverted HCG and LCG signals [9]. By combining the pixel conversion gain setting and the readout circuit setting, three high dynamic range modes can be selected according to the scene.

II. PROPOSED PIXEL AND READOUT CIRCUIT

Figure 2(a) shows a schematic of the proposed area-efficient pixel and readout circuit. The pixel schematic is similar to a conventional LOFIC pixel, except that the MOS capacitor C_S is driven by ΦCS to control its capacitance. When ΦCS is high, C_S is disabled due to the channel being turned off. Conversely, when ΦCS is low, C_S is enabled as the channel is turned on. By implementing the pulse control circuit for ΦCS outside the pixel array, the pixel size can remain as small as that of a conventional LOFIC pixel. The photo-electron conversion gain can be varied by switching ΦSG and ΦCS as described below, where Q_0, C_{FD}, and C_{SG} represent the elementary charge, floating node capacitance, and MOS capacitance of the switching gate, respectively.

(1) In the HCG mode, ΦSG and ΦCS are set to low and high, respectively, as shown in Fig. 2(b), resulting in a conversion gain of Q_0/C_{FD}.

(2) In the MCG mode, both ΦSG and ΦCS are set to high, as shown in Fig. 2(c), resulting in a conversion gain of $Q_0/(C_{FD} + C_{SG})$.

(3) In the LCG mode, ΦSG and ΦCS are set to high and low, respectively, as shown in Fig. 2(d), resulting in a conversion gain of $Q_0/(C_{FD} + C_{SG} + C_S)$. The readout double sampling (DS) circuit operates in the following two modes:

(4) An inverting amplifier mode (INV-AMP) with a high gain of ×8, as shown in Fig. 2(e).

(5) A non-inverting attenuator mode (ATN) with a low gain of ×0.8, as shown in Fig. 2(f).

An attenuation capacitor, $C_{S,ADC}$, for the attenuator is shared with the sampling capacitor of the ADC. There are four practical combinations of the pixel conversion gain and the readout circuit mode: HCG1, HCG2, LCG1, and LCG2, as shown in Table I. The dynamic range can be varied across the three HDR modes, as presented in Table II. HDR1 and HDR3 are suitable for enhancing contrast, while HDR2, which is similar to conventional LOFIC, is more appropriate for scenarios with a wider environmental dynamic range.

The timing diagram of the proposed pixel and readout circuit is shown in Fig. 2(g). First, ΦSG, ΦR, and ΦTG are toggled to reset the PD, C_{FD}, and C_S at t_1, prior to starting the exposure. At the end of exposure, ΦSEL is set to high for a given pixel row, and the pixel reset levels for HCG (V_{RH}) are output from the selected pixel at t_2. At this time, ΦH is turned high but ΦL is turned low in the DS circuit. If ΦSG is set to low, the readout mode is HCG1; if both ΦSG and ΦCS are set to high, the readout mode is HCG2. By toggling ΦTG at t_3, the pixel signal levels for HCG (V_{SH}) is output from the pixel at t_4. The HCG signal, read out from the pixel in a 4T sequence, is inverted and amplified using C_{SH} and C_F, and is then fed to the ADC, as described by

$$V_{ADC}(HCG) = \frac{C_{SH}}{C_F} \cdot (V_{RH} - V_{SH}) + V_b. \quad (1)$$

After this operation, ΦL and ΦSG are set to high, while ΦH is set to low. If ΦCS is set to high, the readout mode is LCG1; if ΦCS is set to low, the readout mode is LCG2. At t_5, the pixel signal levels for LCG (V_{SL}) are directly stored in $C_{S,ADC}$. After ΦR is toggled to reset C_{FD} and C_S, the pixel reset level for LCG (V_{RL}) is output from the pixel array at t_6. The LCG signal, read out from the pixel in a 3T sequence, is non-inverted and attenuated using $C_{S,ADC}$ and C_{ATN}, and is then fed to the ADC, as described by

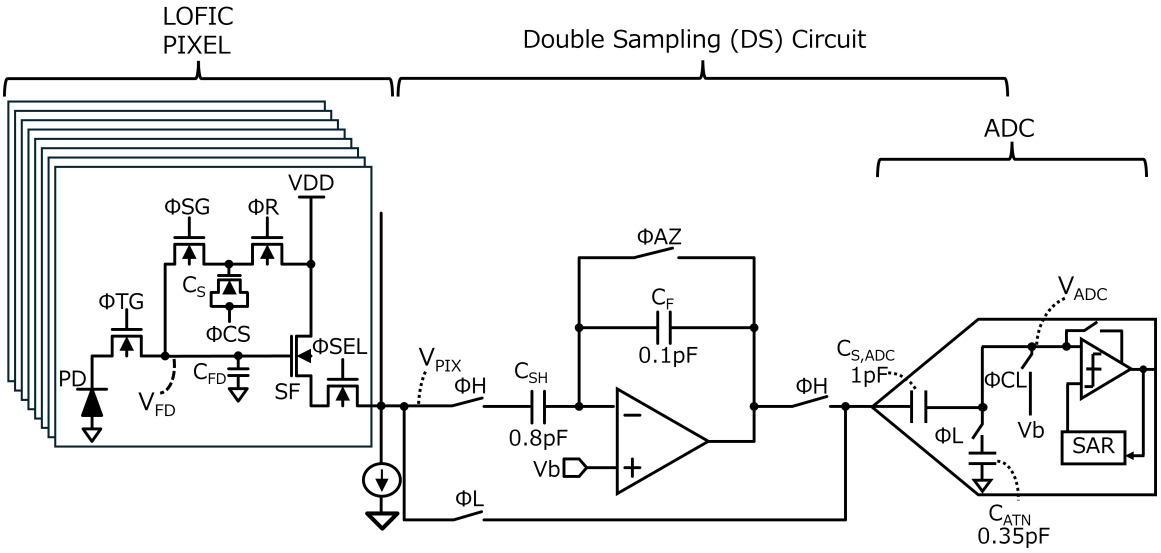
$$V_{ADC}(LCG) = \frac{C_{S,ADC}}{C_{S,ADC} + C_{ATN}} \cdot (V_{RH} - V_{SH}) + V_b. \quad (2)$$

Even though the polarity of the HCG and LCG signals output from the pixel is inverted relative to each other, the polarity of the HCG and LCG signals input to the ADC is aligned because of inverting amplifier and non-inverting attenuator.

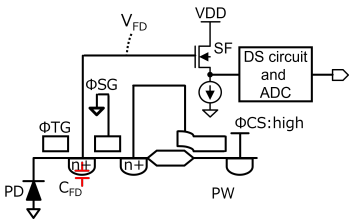
III. FABRICATION AND EVALUATION OF A TEST CHIP

A test chip of the proposed pixel and readout DS circuit for the variable dynamic range CMOS image sensor was fabricated using the 0.18 μm 1P5M CMOS process. A photo of the fabricated test chip is shown in Fig. 3. The test chip includes 648×324 pixels, DS circuit and 10-bit SAR-ADCs with a pitch of 5.6 μm.

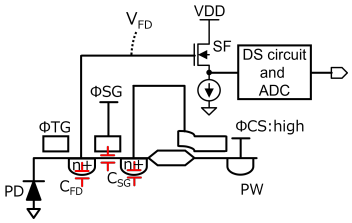
Figure 4 shows the measured input and output characteristics of the HCG1, HCG2, LCG1, and LCG2 signals. The X-axis represents the exposure, and the Y-axis represents the voltage amplitude referred to the ADC input. The HCG1 and HCG2 signals have low noise, thanks to the 4T sequence readout in the pixel and readout circuit amplifier. Although the noise of the LCG1 and LCG2 signals is larger than that of the HCG signals due to 3T sequence readout in the pixel and readout circuit attenuator, the maximum handling charge is large. HDR1 and HDR3 are suitable for darker scenes and brighter scenes, respectively, while HDR2 is optimal for



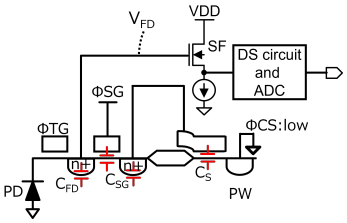
(a) Schematic of the proposed area-efficient pixel and readout circuit



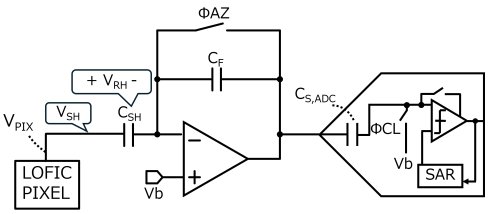
(b) Simplified schematic of the pixel at HCG



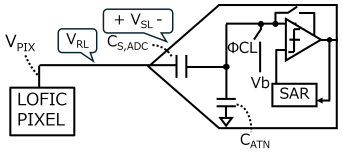
(c) Simplified schematic of the pixel at MCG



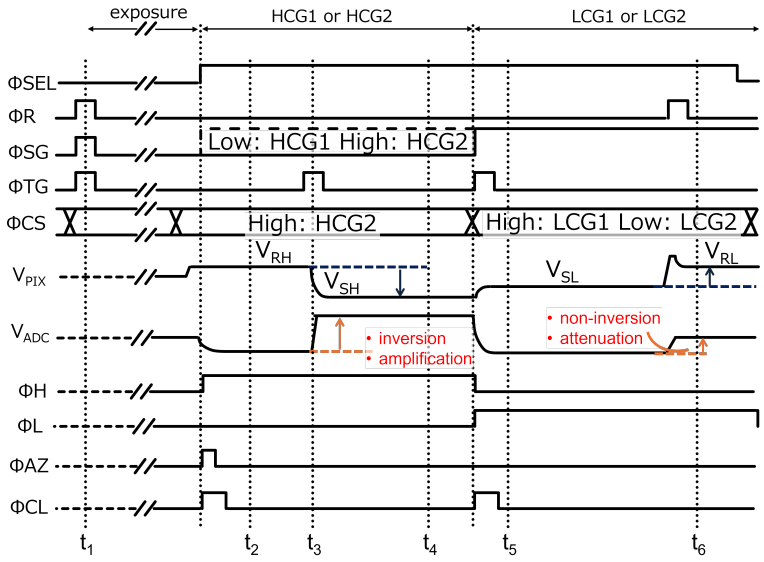
(d) Simplified schematic of the pixel at LCG



(e) Simplified schematic of readout circuit (INV-AMP)



(f) Simplified schematic of readout circuit (ATN)



(g) Timing diagram of the proposed pixel and readout circuit

Fig. 2. Schematic and timing diagram of the proposed area-efficient pixel and readout circuit

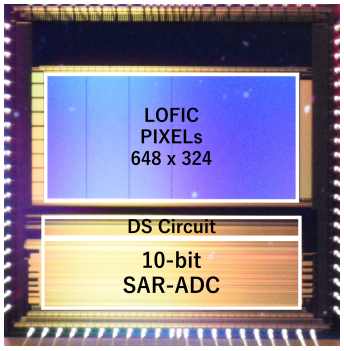


Fig. 3. A photo of the fabricated test chip

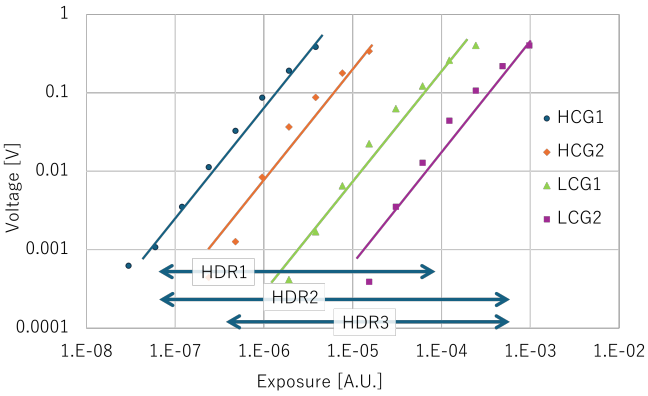


Fig. 4. Measurement result of the fabricated test chip

wider dynamic range environments, such as outdoor scenes with shadows under sunlight. HDR1 and HDR3, with dynamic ranges reduced by 13.3 dB and 18.1 dB, respectively, compared to HDR2, can be selected to enhance image contrast.

The specifications and performance of the proposed pixel and readout circuit are summarized in Table III.

IV. Summary and Future Work

To achieve an HDR CMOS image sensor with a variable dynamic range, an area-efficient LOFIC pixel and a corresponding readout circuit have been proposed. The proposed pixel supports three photo-electron conversion gains by controlling the bottom plate voltage of the overflow MOS capacitor C_S, thus the pixel size can remain as small as that of a conventional LOFIC pixel. The readout DS circuit is composed of an inverting amplifier, a non-inverting attenuator and an ADC. As a result, the dynamic range can be varied across three HDR modes depending on the scene. The highest dynamic range is comparable to that of the conventional LOFIC pixel, while the conversion gain can be reduced by 13.3 dB or 18.1 dB to enhance image contrast.

TABLE III
The specifications and performance of the proposed pixel and readout circuit

Process	0.18 μm 1P5M CMOS
Effective Pixels	648 × 324
Column pitch	5.6 μm
ADC	10 bit
DNL	+3.4 LSB / -0.5 LSB
INL	12.2 LSB

V. Acknowledgments

This work was supported through the activities of VDEC, The University of Tokyo, in collaboration with Cadence Design Systems, with NIHON SYNOPSYS G.K., and with Siemens EDA.

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